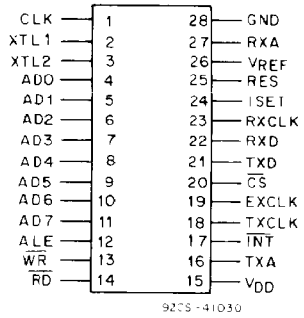
RCA Solid State

CD22212E, CD22212E1, CD22212Q

CMOS Logic Integrated Circuits

Advance Information



CD22212E
TERMINAL ASSIGNMENT

Bell 212A/103 CMOS Single-Chip Modem

Features:

- *One-chip Bell 212A, and 103 standard compatible modem*
- *Full duplex operations at 0-300 BPS (FSK) and 1200 BPS (DPSK)*
- *Pin and software compatible with SSI K221, K222, and K224 one-chip modems*
- *Interfaces directly with standard microprocessors (80C48, 80C51, 8749 typical)*
- *Serial (22-pin DIP) or parallel microprocessor bus (28-pin DIP) for control*
- *Serial port for data transfer*
- *CMOS technology for low power consumption*
- *Both synchronous and asynchronous modes of operation*
- *Call progress, carrier, answer tone and long loop detectors*
- *DTMF generator*
- *Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns*
- *Precise automatic gain control allows 45-dB dynamic range*
- *Available in 22- and 28-pin DIP, and 28-lead PCC packages*
- *Single 12-volt supply*

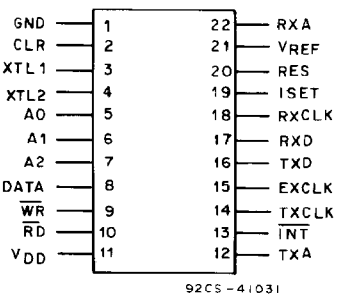
The RCA-CD22212 is a highly integrated single-chip modem IC that provides the functions needed to construct a typical Bell 212A full-duplex modem. Using an advanced CMOS process that integrates analog, digital and switched-capacitor filter functions on a single substrate, the CD22212 offers excellent performance and a high level of functional integration in a single 28-pin or 22-pin configuration.

The CD22212 provides the basic PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a DTMF dialer. This device supports all Bell 212A modes of operation allowing both synchronous and asynchronous communication.

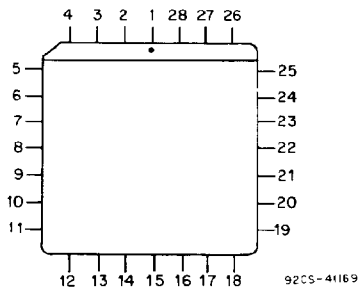
Test features such as analog loop, digital loop, and internal remote digital loopback are provided. Internal pattern generators are also included for self-testing. The CD22212 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communication occurs through a separate serial port only.

Operation

The CD22212 is ideal for use in either free-standing or integral system modem products where full-duplex 1200 BPS data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converters for a typical system.



CD22212E1
TERMINAL ASSIGNMENT



PCC PINOUTS ARE THE SAME AS THE 28-PIN DIP

CD22212Q
TERMINAL ASSIGNMENT

Printed in USA/2-87

File Number **1896**

Asynchronous Mode

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The CD22212 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TxD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TxD pin which must be 1200 bps + 1%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bps ± .01% (± .01% is the crystal tolerance).

The serial data stream from the transmit buffer or the rate converter is then passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2xN+3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed normally first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC converter will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bps. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

Synchronous Mode

The Bell 212A standard defines synchronous operation only at 1200 bps. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TxD must be valid on the rising edge of TxCLK.

TxCLK is an internally derived 1200-Hz signal in internal mode and is connected internally to the RxCLK pin in slave mode. Receive data at the RxD pin is clocked out on the falling edge of RxCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

PSK Modulator/Demodulator

The CD22212 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200-Hz (Originate mode) or 2400-Hz carrier (Answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200-Hz carrier (Answer mode or ALB Originate mode) or a 2400 Hz carrier (Originate mode or ALB Answer mode). The CD22212 uses a phase-locked-loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK Modulator/Demodulator

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225 and 2025 (answer mark and space) are used. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 mode.

Passband Filters and Equalizers

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised cosine frequency response characteristic.

AGC

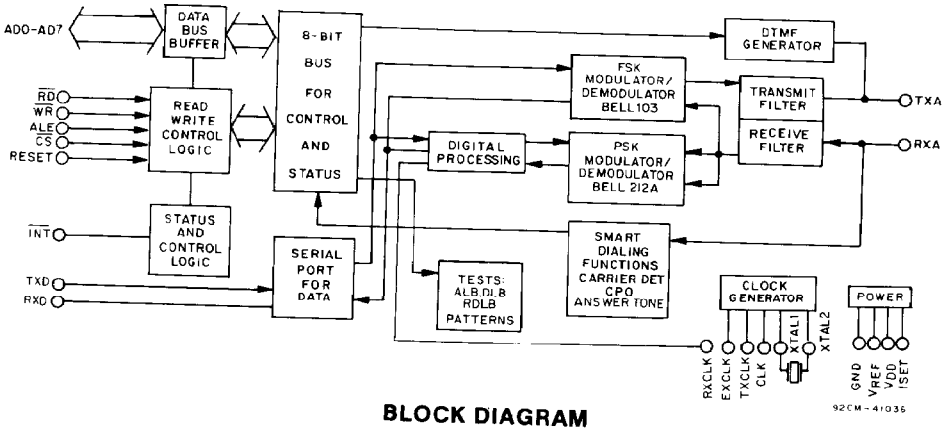
The automatic gain control maintains a signal level at the input to the demodulator which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping, and provides a total dynamic range of > 45 dB.

Parallel Bus Interface

Four 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the A0, A1 and A2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read or write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

Serial Command Interface

The serial command mode allows access to the control and status registers via a serial command port (22-pin version).



BLOCK DIAGRAM

In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of ExCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of ExCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

Special Detect Circuitry

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone, and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 MS ± 6.5 MS. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to a 0.

DTMF Generator

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from a 0 to a 1.

HARDWARE INTERFACE

I/O	Label	28-Pin	22-Pin	Description
POWER				
I	GND	28	1	System Ground
I	VDD	15	11	Power supply input, 12V +10%, -20%. Bypass with .1 uf capacitor to ground
O	Vref	26	21	An internally generated reference voltage for test use. Bypass with .1 uf capacitor to ground.
I	Iset	24	19	Chip current reference. Sets bias current for op-amps. The chip currrent is set by connecting this pin to VDD through a 4 MΩ resistor. Iset should be bypassed to GND with a .1 uf capacitor.
MICROPROCESSOR INTERFACE				
I	ALE	12	-	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
I/O	AD0-AD7	4-11	-	Address/data bus. These bidirectional tri-state multiplexed lines carry infromation to and from the internal registers.
I	$\overline{CS}$	20	-	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
O	CLK	1	2	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16x1200 Hz for use as a baud rate clock. The pin defaults to the crystal frequency on reset.
O	$\overline{INT}$	17	13	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occured. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
I	$\overline{RD}$	14	-	Read. A "low" requests a read of the CD22212 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low".
I	RESET	25	20	Reset. An active signal ("high") on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be set to zero. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a .1µf capacitor to VDD.
I	$\overline{WR}$	13	-	Write. A "low" on this informs the CD22212 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").
RS-232 INTERFACE				
I	ExCLK	19	15	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of ExCLK is used to strobe synchronous DPSK transmit data available on the TxD pin. Also used for serial control interface.

HARDWARE INTERFACE (Continued)

I/O	Label	28-Pin	22-Pin	Description
O	RxCLK	23	18	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RxCLK can be used to latch the valid output data. RxCLK will be active as long as a carrier is present.
O	RxD	22	17	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RxCLK when in synchronous mode.
O	TxCLK	18	14	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TxD pin. Data must be provided so that valid data is available on the rising edge of the TxCLK clock. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TxCLK is phase locked to the ExCLK pin. In Slave Mode TxCLK is phase locked to the RxCLK pin. TxCLK is always active.
I	TxD	21	16	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TxCLK clock. In asynchronous modes (1200 BPS or 300 baud) no clocking is necessary. 1200 BPS data must be 1200 bps +1%, -2.5%

ANALOG INTERFACE

I	RxA	27	22	Received modulated analog signal input from the phone line.
O	TxA	16	12	Transit analog output to the phone line.
I	XTAL1 XTAL2	2 3	3 4	These pins are for the internal crystal oscillator requiring a 11.0592 MHz crystal. XTAL1 can also be TTL-driven from an external clock.

SERIAL INTERFACE

I	AO-A2	-	5-7	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
I/O	Data	-	8	Serial Control Data. Data for a read/write operation is clocked in or out on the falling ede of the ExCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
I	$\overline{RD}$	-	10	Read. A "low" on this input informs the CD22212 that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of ExCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
I	$\overline{WR}$	-	9	Write. A "low" on this input informs the CD22212 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of ExCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-Pin version, the pins AD0-AD7, ALE, and $\overline{CS}$ are removed and replaced with the pins A0, A1, A2 and DATA . Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control version is provided by floating ALE and $\overline{CS}$ or by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2.

Register Descriptions

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the CD22212 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer tone and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER	ADDRESS A2-A0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	MODE 0	TRANSMIT ENABLE	ORIGINATE /ANSWER
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN BIT 1	TRANSMIT PATTERN BIT 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RxD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF 1	DTMF 0
CONTROL REGISTER 2 CR4	100	THESE REGISTER LOCATIONS ARE RESERVED FOR							
CONTROL REGISTER 3 CR5	101	USE BY FUTURE TYPES							
ID REGISTER ID	110	0	0						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	AD2-AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE /ANSWER
				0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYCH 8 BIT/CHAR 0101=ASYCH 9 BITS/CHAR 0110=ASYCH 10 BITS/CHAR 0111=ASYCH 11 BITS/CHAR 1100=FSK				0=SQUELCH ANALOG 1=ENABLE ANALOG	0=ANSWER 1=ORGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		ENABLE DETECT INTERRUPT 1=ON 0=OFF	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16X1200 HZ OUTPUT AT CLK PIN	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0
		RXD PIN 1=TRI STATE 0=NORMAL		1=ON 0=OFF	1=TX DTMF 0=DATA	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS OVERIDES OTHER TRANSMIT CODES			
ID REGISTER ID	110	ID BIT 1	ID BIT 0						
		00 212 10 XXX 01 221 11 XXX (RESERVED FOR FUTURE TYPES)							

REGISTER BIT DESCRIPTION

CONTROL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
CR0			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE ANSWER

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Originate Answer	0	Selects answer mode (Transmit in high band, receive in low band)
		1	Selects originate mode (Transmit in low band, receive in high band)
D1	Transmit Enable	0	Disables transmit output at TXA
		1	Enables transmit output at TXA NOTE: Answer tone and DTMF TX control require TX enable
D2, D3, D4, D5	Transmit Mode	D5 D4 D3 D2	
		0000	Selects power down mode----all functions disabled except digital interface
		0001	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0010	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0011	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0100	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0101	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit)
		0110	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0111	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, 1 stop bit).
		1100	Selects FSK operation.

REGISTER BIT DESCRIPTION (Cont'd)

CONTROL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
CR1	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS. SCRAMB.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D1	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		1 0	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		0 1	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 19.2 KHz (16 x 1200 Hz) output at CLK pin.
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enbles $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect interrupt is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D6, D7	Transmit Pattern	00	Selects normal data transmission as controlled by the input to the TXD pin.
		01	Selects an alternating mark/space transmit pattern for modem testing.
		10	Selects a constant mark transmit pattern.
		11	Selects a constant space transmit pattern.

REGISTER BIT DESCRIPTION (Cont'd)

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR			RECEIVE DATA	UNSCR. MARKS	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0 1	Indicates normal received signal. Indicates low received signal level (< -38 dBm).
D1	Call Progress Detect	0 1	No call progress tone detected. Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Answer Tone Received	0 1	No answer tone detected. Indicates detection of 2225 Hz answer tone. The device must be in originate mode for detection of answer tone in normal operation.
D3	Carrier Detect	0 1	No carrier detected in the receive channel. Indicated carrier has been detected in the receive channel.
D4	Unscr Mark (Unscrambled Mark)	0 1	No unscrambled mark. Indicated detection of unscraambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 msec.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

REGISTER BIT DESCRIPTION (Cont'd)

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR	RxD OUTPUT CONTR		TRANS. ANSWR TONE	TRANS. DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0,D1,D2,D3	DTMF	0000 to 1111	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, Bit D1) is set. Tone encoding is shown below.
D4	TX DTMF (Transmit DTMF)	0 1	Disabled DTMF. Activates DTMF. The selected DTMF tones are transmitted continuously when this bit(with Transmit Enable, CR0-D1) is high. Tx DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer tone)	0 1	Disables answer tone generator. Enables answer tone generator. A 2225 Hz answer tone will be transmitted continously when the transmit enable bit is set. The device must be in answer mode.
D7	RXD Open	0 1	Enables RXD pin. Received data will be output on RXD. Disables RXD pin. The RXD pin reverts to a high impedance with internal pull-up resistor.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1209
*	1	0	1	1	941	1336
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID	ID BIT 1	ID BIT 0						

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 0 0 0 1 1 0 1 1	 CD22212 CD22221 Reserved for Future Types Reserved for Future Types

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C TO 85°C, VDD = RECOMMENDED RANGE UNLESS OTHERWISE NOTED)

PARAMETER	RATING	UNITS
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Output Current	±3	mA

Notes: 1. All inputs and outputs are protected from static charge using built-in industry standard protection devices.
2. All outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD, SUPPLY VOLTAGE		9.6	12	13.2	V
VIH, INPUT HIGH VOLTAGE					
RESET, XTAL 1		3.0		VDD	V
ALL OTHER INPUTS		2.0		VDD	V
VIL, INPUT LOW VOLTAGE		0		0.8	V
IOH, OUTPUT HIGH CURRENT		-0.4			mA
IOL, OUTPUT LOW CURRENT				1.6	mA
TA, OPERATING FREE -AIR TEMPERATURE		-40		85	°C
EXTERNAL COMPONENT (REFER TO APPLICATION SECTION FOR PLACEMENT)					
VREF BYPASS CAPACITOR	EXTERNAL TO GND	0.1			µF
BIAS SETTING RESISTOR	PLACED BETWEEN VDD AND ISET PINS	3.8	4	4.2	MΩ
ISET BYPASS CAPACITOR	EXTERNAL TO GND	0.1			µF
VDD BYPASS CAPACITOR	EXTERNAL TO GND	0.1			µF
INPUT CLOCK VARIATION	11.0592 MHz Clock	-0.01		+0.01	%

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to +85°C, VDD = 12V + 10% - 20% UNLESS OTHERWISE NOTED)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, SUPPLY CURRENT	ISET RESISTOR = 3.9MΩ				
IDDA, ACTIVE	CLK = 11.0592 MHZ		15	25	mA
IDD1, POWER-DOWN	CLK = 11.0592 MHZ		8	11	mA
IDD2, POWER-DOWN	CLK = 19.200 KHZ		6	9	mA
IIH, INPUT HIGH CURRENT	VI - VIH MAX			100	µA
IIL, INPUT LOW CURRENT	VI - VIL MIN	-200			µA
VOH, OUTPUT HIGH VOLTAGE	IO = IOH MIN	2.4		4.75	V
VOL, OUTPUT LOW VOLTAGE	IO = IOL MAX			0.4	V
VOL, CLK OUTPUT	IO = 0.8 mA			0.4	V
RESET PULL-DOWN CURRENT	RESET = VDD	5		50	µA

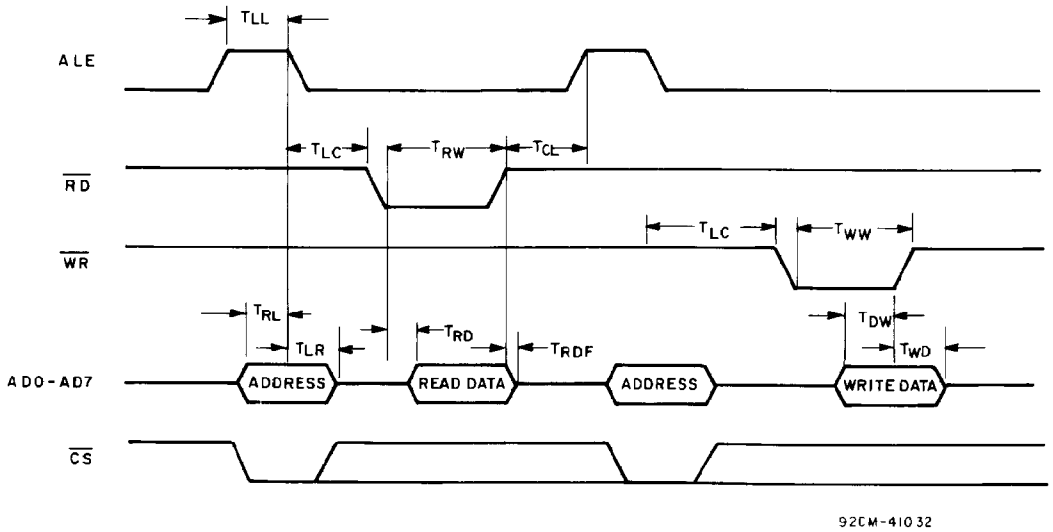
DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = 12V + 10% - 20% UNLESS OTHERWISE NOTED)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
PSK MODULATOR CARRIER SUPPRESSION	MEASURED AT TXA	55			dB
OUTPUT AMPLITUDE	TX SCRAMBLED MARKS	-10.8	-10.0	-9.2	dBm0
FSK MOD/DEMOD OUTPUT FREQ. ERROR	CLK = 11.0592 MHZ	-0.35		0.35	%
TRANSMIT LEVEL	XMIT DOTTING PATTERN	-10.8	-10.0	-9.2	dBm0
HARMONIC DISTORTION	THD IN 700-2900 HZ BAND @ TXA			-29	dB
OUTPUT BIAS DISTORTION	XMIT DOTTING PATTERN IN ALB @ RXD	-5		+5	%
TOTAL OUTPUT JITTER	RANDOM INPUT IN ALB @ RXD	-12		12	%
DTMF GENERATOR					
FREQ. ACCURACY		-.25		.25	%
OUTPUT AMPLITUDE	LOW BAND	-10		-8	dBm0
OUTPUT AMPLITUDE	HIGH BAND	-8		-6	dBm0
TWIST	HIGH BAND TO LOW BAND	1.0	2.0	3.0	dB
LONG LOOP DETECT		-41		-32	dBm0
CALL PROGRESS DETECTOR					
DETECT LEVEL	2-TONE IN 350-620HZ BAND	-34		0	dBm0
REJECT LEVEL	2-TONE IN 350-620HZ BAND			-42	dBm0
DELAY TIME	-70 dBm0 to -30 dBm0 STEP			30.0	ms
HOLD TIME	-30 dBm0 to -70 dBm0 STEP			30.0	ms
HYSTERESIS		2			dB
CARRIER DETECT					
THRESHOLD	DPSK or FSK RANDOM DATA	-51		-43	dBm0
DELAY TIME	-70 dBm0 to -30 dBm0 STEP	21		30	ms
HOLD TIME	-30 dBm0 to -70 dBm0 STEP	7		30	ms
ANSWER TONE DETECTOR					
DETECT LEVEL	IN FSK MODE, SINGLE-TONE, 2225HZ	-51		-41	dBm0
DELAY TIME	-70 dBm0 to -30 dBm0 STEP	15		45	ms
HOLD TIME	-30 dBm0 to -70 dBm0 STEP	7		30	ms
OUTPUT SMOOTHING FILTER OUTPUT LOAD	TXA PIN; FSK SINGLE TONE OUT FOR THD= -50 dB IN .3 TO 3.4 KHZ BAND	10			KΩ
SPURIOUS FREQ. COMP.	FREQ. 80 KHZ			-39	dBm
CLOCK NOISE	TXA PIN; 76.8 KHZ			3	mVrms
OUTPUT IMPEDANCE	TXA PIN		200	300	Ω

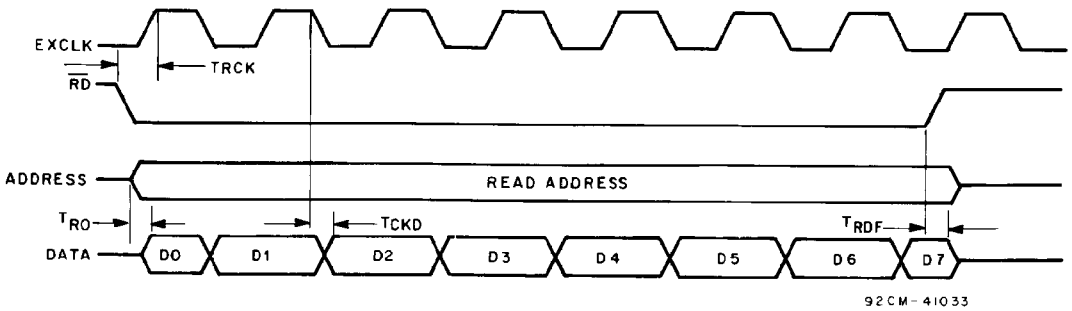
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
CARRIER VCO					
CAPTURE RANGE	ORIGINATE OR ANSWER	-10	±20	10	Hz
CAPTURE TIME	-10 Hz to +10 Hz CARRIER FREQ. CHANGE ASSUM.		40	100	ms
DIBIT CLOCK RECOVERY DIGITAL OSCILLATOR					
CAPTURE RANGE	% OF FREQUENCY CENTER FREQUENCY CENTER AT 1200 HZ	+0.25		-0.25	%
DATA DELAY TIME	ANALOG DATA IN AT RXA PIN TO RECEIVE DATA VALID AT RXD PIN		30	50	ms
DYNAMIC RANGE	REFER TO PERF. CURVES		44		dB
CAPACITANCE					
INPUTS				10	pf
XTAL1, XTAL2		20	30	40	pf
CLK				15	pf
TIMING (REFER TO TIMING DIAGRAM)					
Tal	ADDR. BEFORE LATCH	30			ns
Tla	ADDR. HOLD AFTER LATCH	20			ns
Tlc	LATCH TO $\overline{RD}/\overline{WR}$ CONTROL	40			ns
Tcl	$\overline{RD}/\overline{WR}$ CONTROL TO LATCH	10			ns
Trd	DATA OUT FROM $\overline{RD}$	0		160	ns
Tll	ALE WIDTH	60			ns
Trdf	DATA FLOAT AFTER READ	0		80	ns
Trw	READ WIDTH	200		5000	ns
Tww	WRITE WIDTH	140		5000	ns
Tdw	DATA SETUP BEFORE WRITE	150			ns
Twd	DATA HOLD AFTER WRITE	20			ns
Trck	CLK AFTER READ (22-PIN)	500			ns
Tckd	DATA OUT AFTER CLK			200	ns
Tckw	WRITE AFTER CLK	1			µs
Tdck	DATA SETUP BEFORE CLK	150			ns

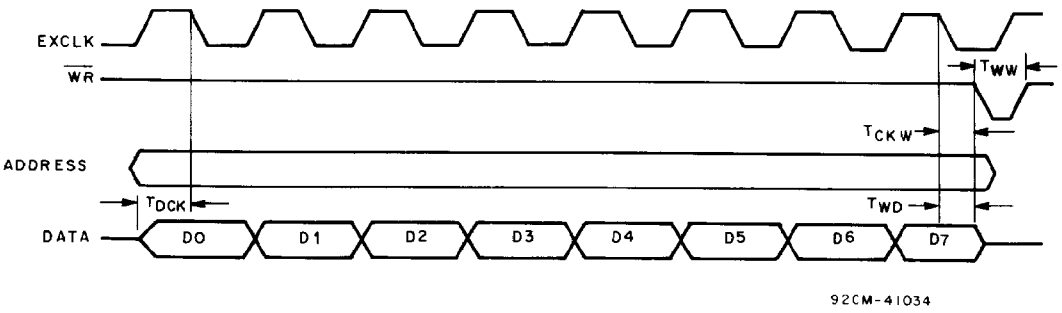
Note: All parameters expressed in units of dBm0 assume a hybrid loss of -9 dB in the transmit path and a gain of 11 dB in the receive path from the 600Ω line with the line terminated with 600Ω. See the Basic Box Modem diagram in the Applications section for the recommended DAA design..



BUS TIMING DIAGRAM



READ TIMING DIAGRAM

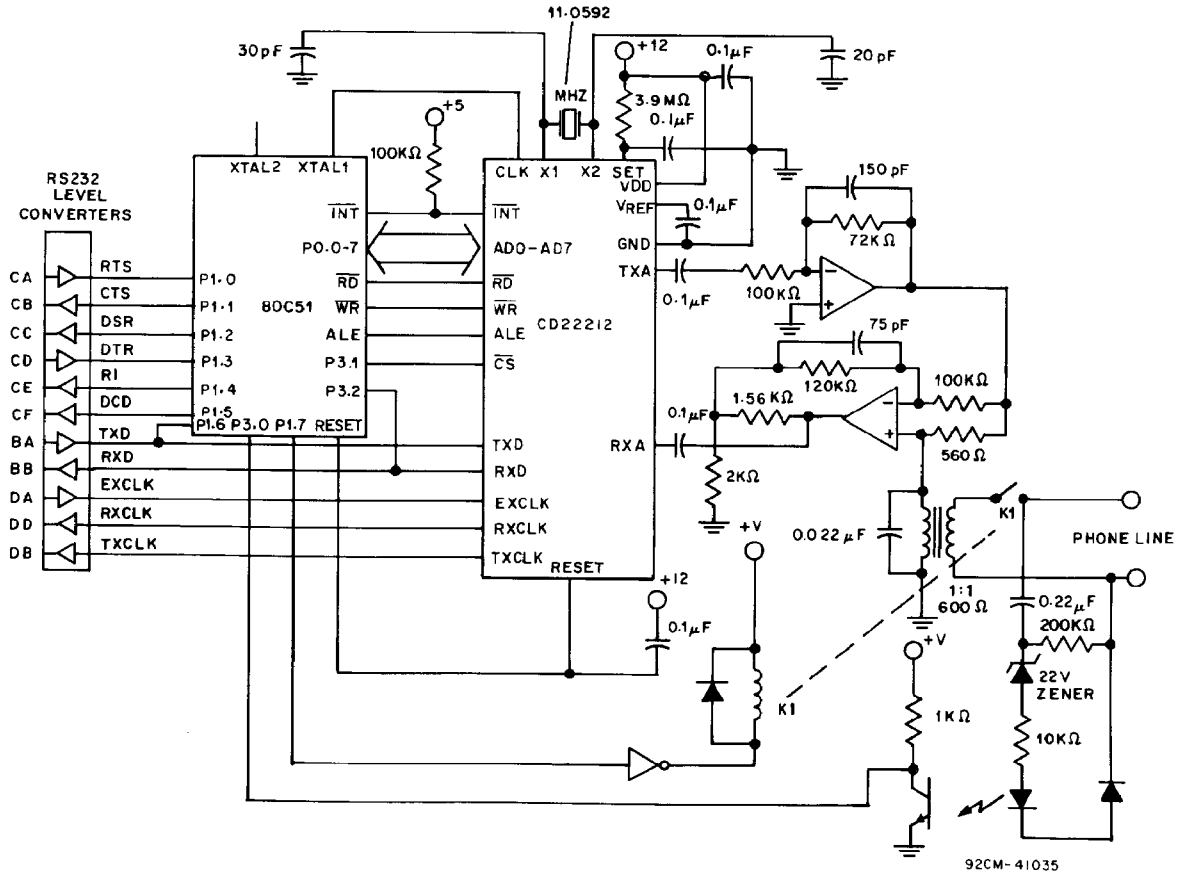


WRITE TIMING DIAGRAM

Application

The CD22212 is designed to be used in conjunction with a microprocessor and RS-232 serial lines or parallel bus interface, and a DAA phone line interface to function as a typical intelligent modem. The CD22212 interfaces directly with 8048/8051 family microprocessors for this purpose. Shown below is a basic modem circuit for the stand-alone modem (self-contained box), which functions as described in the following section.

A typical intelligent modem consists of the mod/demod block, phone line and terminal interfaces, and a dedicated control microprocessor as shown in the block diagram. The CD22212 has two buses–a parallel or serial bus for control or status monitoring; and a serial bus for data transfer. Either a serial or parallel interface can be used to transfer data (and commands) between the modem and terminal, but the actual data path is through the serial port. A dedicated microprocessor monitors the TXD line from the terminal, interprets commands in the data stream and takes control action in response to these commands by using the CD22212 control bus to access its four internal registers. The received data path is monitored by passing received data to the control processor to allow sending messages back to the terminal for status indication. The mod/demod block performs the Bell 212A communications link, which includes asynchronous buffer/debuffer functions at 1200 bps, scrambler/descrambler, and synchronous DPSK 1200 bps and the Bell 103 FSK 0-300 bps modulation/demodulation. DTMF dialing capability allows the modem to dial its own calls. Call progress detection expands this capability by giving the modem the ability to detect dial tone, busy signal, or ringback, and to change its calling action in response to these detected signals. An FCC-approved DAA section completes the modem by providing a connection to the dial-up phone line.



BASIC BOX MODEM

PERFORMANCE CHARACTERISTICS

The CD22212 was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The curves in this section define expected performance under various line conditions and with disturbances typical of those encountered when using PSTN lines for data transmission. Test data was taken using an AEA Electronics "Autotest I" modem test set and line simulator operating under computer control. All tests were run full-duplex with a Concord Data Systems 224 as the reference modem. A 511 pseudo-random bit pattern was used with $1x10^6$ bits transmitted for each data point. Noise is C-message weighted and all S/N ratios reflect total power measurements similar to the V.56 measurement specification.

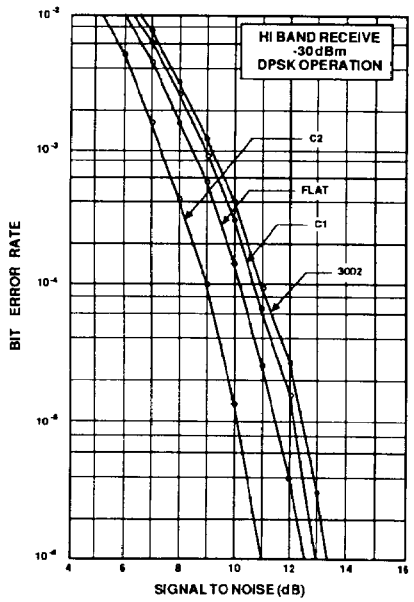
BER vs. S/N: This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities. High-band receive data is typically better than low band due to the inherent design of PSK modems.

Ideal Receivers: The modem transmitter is a much simpler function to implement than the receiver. Because of this, it is generally assumed that only the receiver needs to be analyzed. In practice, this is not the case and transmitter variations unit-to-unit can effect overall performance. This curve indicates the effect of the transmitter on the high-band receive performance of an ideal receiver.

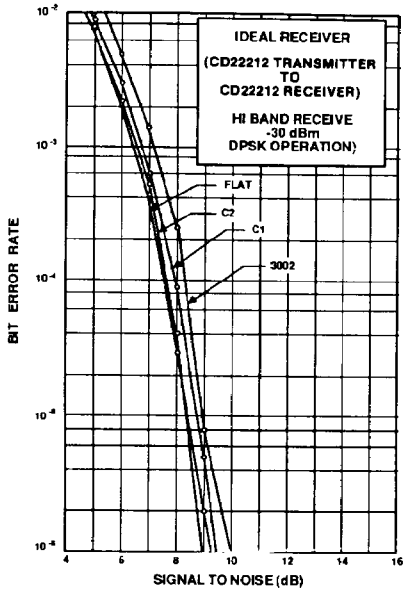
BER vs. Receive Level: This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36-dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10^{-4} BER point is a measure of the dynamic range.

BER vs. Phase Jitter: PSK modulation is sensitive to phase jitter. Modems using this technique need to be as tolerant as possible of phase jitter on the line. Relatively flat curves indicate minimal performance degradation when phase jitter is encountered on the line.

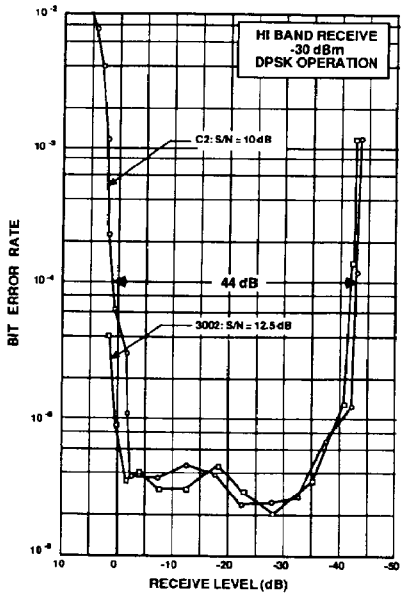
BER vs. Carrier Offset: This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10 Hz. The Bell network specifications allow as much as 7-Hz offset, and the CCITT specs require modems to operate with 7 Hz of offset.



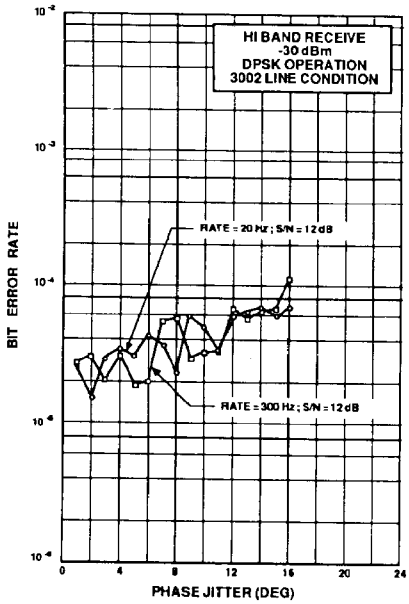
BIT ERROR RATE vs S/N



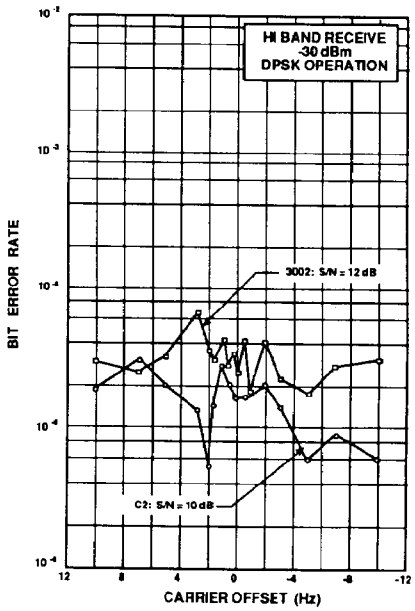
BIT ERROR RATE vs S/N



BIT ERROR RATE vs RECEIVE LEVEL

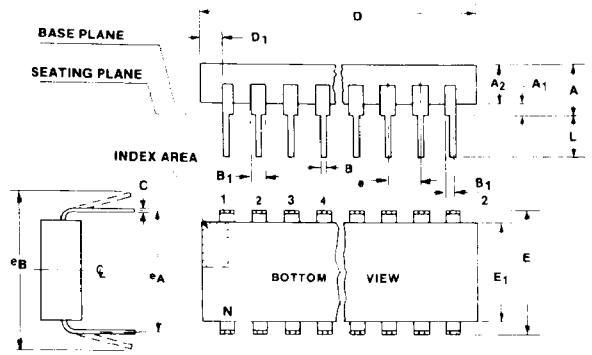


BIT ERROR RATE vs PHASE JITTER



BIT ERROR RATE vs CARRIER OFFSET

DIMENSIONAL OUTLINES



Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(E) SUFFIX (JEDEC MS-010-AA)
22-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.050	1.120	26.67	28.44	4
D_1	0.005	—	0.13	—	12
E	0.390	0.425	9.91	10.79	5
E_1	0.330	0.380	8.39	9.65	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.400 BSC		10.16 BSC		9
e_B	—	0.500	—	12.70	10
L	0.115	0.160	2.93	4.06	9
N	22		22		11

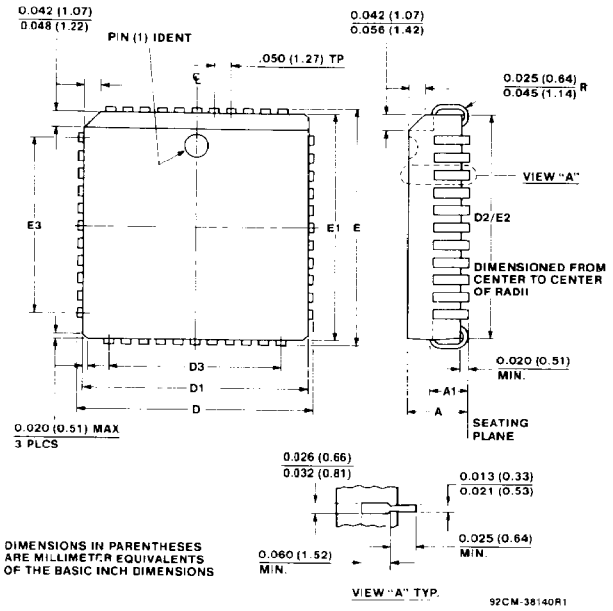
92CS-39999

(E) SUFFIX (JEDEC MS-011-AB)
28-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.1	39.7	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	28		28		11

92CS-40001

Plastic Chip-Carrier (PCC) Package



(Q) SUFFIX (JEDEC MO-047AB)
28-Lead Square Surface-Mount
Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.165	0.180	4.20	4.57	
A_1	0.090	0.120	2.29	3.04	
D	0.485	0.495	12.32	12.57	
D_1	0.450	0.456	11.430	11.582	2
D_2	0.390	0.430	9.91	10.92	1
D_3	0.300 REF		7.62 BSC		
E	0.485	0.495	12.32	12.57	
E_1	0.450	0.456	11.430	11.582	2
E_2	0.390	0.430	9.91	10.92	1
E_3	0.300 REF		7.62 BSC		
N	28		28		3

92CM-39435

NOTES:
1. **To be determined at seating plane.**
2. **Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.254 mm/0.010 in.**
3. **"N" is the number of terminal positions.**
4. **Controlling dimensions: inch.**
5. **All leads at seating plane to be coplanar within 0.004 in.**

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**
   All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525, "Guide to Better Handling and Operation of CMOS Integrated Circuits."
2. **Operating**

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 1 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

ORDERING INFORMATION

Device No.	Control Interface	No. of Leads	Package
CD22212E	Parallel	28	DIP
CD22212E1	Serial	22	DIP
CD22212Q	Parallel	28	PCC

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices," Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.